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- ☐ 1. **A 40-43-Gb/s clock and data recovery IC with integrated SFI-5 1:16 demul technology**
 Ong, A.; Benyamin, S.; Cancio, J.; Conditto, V.; Labrie, T.; Qinghung Lee; Matti D.K.; Shahani, A.; Xiaomin Si; Hai Tao; Tarsia, M.; Wong, W.; Min Xu;
[Solid-State Circuits, IEEE Journal of](#)
 Volume 38, Issue 12, Dec 2003 Page(s):2155 - 2168
 Digital Object Identifier 10.1109/JSSC.2003.818565
[AbstractPlus](#) | Full Text: [PDF](#)(1583 KB) IEEE JNL
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- ☐ 2. **Equalization and clock recovery for a 2.5-10-Gb/s 2-PAM/4-PAM backplan cell**
 Zerbe, J.L.; Werner, C.W.; Stojanovic, V.; Chen, F.; Wei, J.; Tsang, G.; Kim, D W.F.; Ho, A.; Thrush, T.P.; Kollipara, R.T.; Horowitz, M.A.; Donnelly, K.S.;
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 Volume 38, Issue 12, Dec 2003 Page(s):2121 - 2130
 Digital Object Identifier 10.1109/JSSC.2003.818572
[AbstractPlus](#) | Full Text: [PDF](#)(2168 KB) IEEE JNL
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- ☐ 3. **A 10-GB/s SONET-compliant CMOS transceiver with low crosstalk and in**
 Werker, H.; Mechnig, S.; Holuigue, C.; Ebner, C.; Mitteregger, G.; Romani, E.; T.; Moyal, M.; Vena, M.; Melodia, A.; Fisher, J.; de Mercey, G.L.G.; Geib, H.;
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[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(1536 KB) IEEE JNL
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- ☒ 4. **Clock and data recovery with adaptive loop gain for spread spectrum Ser**
 Ming-ta Hsieh; Sobelman, G.E.;
[Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on](#)
 23-26 May 2005 Page(s):4883 - 4886 Vol. 5
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[AbstractPlus](#) | Full Text: [PDF](#)(296 KB) IEEE CNF
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5. **A low jitter, low power, CMOS 1.25-3.125Gbps transceiver**

- ☐ Younis, A.; Boecker, C.; Hossain, K.; Abughazaleh, F.; Das, B.; Yiqin Chen; R. S.; Grung, B.;
Solid-State Circuits Conference, 2001. ESSCIRC 2001. Proceedings of the 27th 18-20 Sept. 2001 Page(s):121 - 124
[AbstractPlus](#) | Full Text: [PDF](#)(1016 KB) [IEEE CNF](#)
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- ☐ 6. **A 10Gb/s/ch 50mW 120/spl times/130/spl mu/m/sup 2/ clock and data rec**
Kaeriyama, S.; Mizuno, M.;
Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC. 2003. International
2003 Page(s):70 - 478 vol.1
Digital Object Identifier 10.1109/ISSCC.2003.1234211
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- ☐ 7. **Architecture and methodology of a SoPC with 3.25Gbps CDR based SERI dynamic phase alignment**
Venkata, R.; Wong, W.; Tran, T.; Chan, V.; Hoang, T.; Lui, H.; Ton, B.; Shumu Lee; Shoujun Wang; Huy Ngo; Kabani, M.; Maruri, V.; Tin Lai; Tam Nguyen; Zi Luo; Toan Nguyen; Asaduzzaman, K.; Maangat, S.; Lam, J.; Patel, R.;
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- ☐ 8. **A 62.5 Gb/s multi-standard SerDes IC**
Partovi, H.; Evans, B.; Wilson, T.; Shelton, S.; Naviasky, E.; Sanjeevi, E.; Wen Gopalakrishnan, K.; Chokkalingam, S.; Thompson, H.; Casas, M.; Lingting Ye; Yujing Qiu; Williams, M.; James, J.; Baldiserotto, A.; White, S.; Williams, S.; Gray, T.;
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- ☐ 9. **A UTMI-compatible physical-layer USB2.0 transceiver chip**
Nam, J.-J.; Kim, Y.-J.; Choi, K.-H.; Park, H.-J.;
SOC Conference, 2003. Proceedings. IEEE International [Systems-on-Chip] 17-20 Sept. 2003 Page(s):309 - 312
Digital Object Identifier 10.1109/SOC.2003.1241532
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- ☒ 10. **A compact phase interpolator for 3.125G Serdes application**
Yueming Jiang; Piovaccari, A.;
Mixed-Signal Design, 2003. Southwest Symposium on 23-25 Feb. 2003 Page(s):249 - 252
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- ☐ 11. **Effects of amplitude modulation in jitter tolerance measurements of com devices**
Ishida, M.; Yamaguchi, T.J.; Soma, M.; Musha, H.;
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☐ **12. 1.5 Gbps, 5150 ppm spread spectrum SerDes PHY with a 0.3 mW, 1.5 Gb/s for serial ATA**

Sugawara, M.; Ishibashi, T.; Ogasawara, K.; Aoyama, M.; Zwerger, M.; Glowinski, Y.; Yanagita, T.; Fukaishi, M.; Shimoyama, S.; Noma, T.;

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Shuguiang Li; Junyan Ren; Lianxing Yang; Fan Ye; Zhang, Y.M.M.;

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☐ **14. Digital serial communication device testing and its implications on autonomous equipment architecture**

Cai, Y.; Warwick, T.P.; Rane, S.G.; Masserrat, E.;

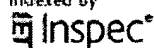
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 Imai, Y.; Sano, E.; Nakamura, M.; Ishihara, N.; Kikuchi, H.; Ono, T.;
Microwave Theory and Techniques, IEEE Transactions on
 Volume 41, Issue 5, May 1993 Page(s):745 - 751
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- ☐ 2. **A UTMI-compatible physical-layer USB2.0 transceiver chip**
 Nam, J.-J.; Kim, Y.-J.; Choi, K.-H.; Park, H.-J.;
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